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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/707,521	11/06/2000	Amelia C. Luna	SONY-50P3845	9729

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EXAMINER	
REKSTAD, ERICK J	

ART UNIT	PAPER NUMBER
2613	

DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/707,521	LUNA ET AL.	
	Examiner	Art Unit	
	Erick Rekstad	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a final rejection for application no. 09/707,521 in response to applicants after final amendment filed on 8/17/2004.

Response to Arguments

Applicant's arguments, see Page 12 of After Final, filed 8/17/2004, with respect to the rejection(s)of claim(s) 1-37 under US Patent 6,172,621 to Iwata have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of 'Low-Power Video Encoder/Decoder Chip Set for Digital VCR's' by Hasegawa et al.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 6-8, 10-12, 15-20, 22, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over 'Low-Power Video Encoder/Decoder Chip Set for Digital VCR's' by Hasegawa et al in view of US Patent 5,845,083 to Hamadani et al.

[claims 1-3, 6, 8, 18-20, 22, 29]

As shown in Figure 1, Hasegawa teaches the DV decoder containing the steps of unpacking, VLD, Dequantize, IDCT, and Deshuffling. Hasegawa further teaches the unpacking process is performed while the VLD is being performed (Page 1784 section D, Fig. 9). Hasegawa further teaches the main difference between DV and MPEG is the

shuffling and packing steps (Page 1781 Section B). Hasegawa teaches the Shuffling step allows for writing and reading at the same time (Page 1784 Section C). Hasegawa does not specifically teach the process of VLD and decompression at the same time. As shown in Figure 5, Hamadani teaches a MPEG compliant decoder containing a control (158) for allowing the VLD (148) and decompression (152 and 154) to operate simultaneously (Col 1 Lines 5-10, Col 7 Lines 13-31). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the system of Hasegawa with the MPEG decoder of Hamadani as DV and MPEG are similar encoding processes.

[claims 7 and 28]

As required by claim 7, Hasegawa teaches the variable length coding format comprises a Huffman code format (Page 1782-1783 Section E, Fig. 5). Hamadani also teaches the variable length coding format comprises a Huffman code format (Col 6 Lines 15-18).

[claims 10-12, 15-17]

Hasegawa and Hamadani teach the method and apparatus of claims 1-3, 5-7, 18-20, and 22. Hasegawa does not teach the use of a computer readable medium for storing the method. Hamadani does not teach the computer readable medium for storing the method. It is well known in the art to replace hardware based apparatuses with a general purpose computer and computer readable medium providing the method in order to provide cost affective changes and upgrades to the system (Official Notice). It would have been obvious to one of ordinary skill in the art at the time of the invention

to replace the apparatus of Hasegawa and Hamadani with computer readable medium in order to provide a general purpose computer the method to perform the decoding process (Official Notice).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa and Hamadani as applied to claim 1 above, and further in view of US Patent 6,389,171 to Washington.

[claim 9]

Hasegawa and Hamadani teach the system of claim 1. Hasegawa teaches the use of DV encoding/decoding as shown above for claim 1. Hasegawa further teaches that DV and MPEG are similar compression formats (Page 1781 Section B). Hasegawa does not specifically teach the use of the decoder with MPEG streams. As shown in Figure 5, Hamadani teaches a MPEG compliant decoder containing a control (158) for allowing the VLD (148) and decompression (152 and 154) to operate simultaneously (Col 1 Lines 5-10, Col 7 Lines 13-31). Washington teaches that MPEG and DV are well known digital data formats that use Huffman coding to encode digital data in an ever smaller space in an effort to make digital cameras and digital camcorders more attractive for the users (Col 1 Lines 32-38, Lines 57-67). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the digital video data formats MPEG or DV, which both use Huffman encoding, with the decoder of Hasegawa and Hamadani in order to provide a decoder for the increasingly popular encoding techniques used in digital camcorders, as taught by Washington.

Claims 4, 5, 13, 14, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa and Hamadani in view of US Patent 6,496,199 to Peng et al.

[claims 4, 5, and 27]

Hasegawa and Hamadani teach the use of a digital video decoder containing a preparser, vld, and a de-shuffler as shown above for claims 1, 10 and 18. They do not teach the use of a Very Long Instruction Word (VLIW) processor. Peng teaches the use of a VLIW CPU to control a system-on-a-chip video decoder in order to implement an advanced multimedia system at an affordable cost and with a smaller footprint (Col 1 Lines 50-55, Lines 59-63). The VLIW CPU contains an on-chip instruction cache that could obviously be used to store instructions on preparsing video data. The steps of the decoder are obviously controlled under time sharing criteria because a real-time digital video decoder is required to perform the decoding steps in a specific amount of time. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the decoding method of Hasegawa and Hamadani with the system of Peng in order to produce an affordable and small advanced multimedia system.

[claims 13 and 14]

As shown above Hasegawa, Hamadani and Peng teach the method and apparatus of claims 4, 5, and 27. Hasegawa does not teach the use of a computer readable medium for storing the method. Hamadani does not teach the computer readable medium for storing the method. It is well known in the art to replace hardware based apparatuses with a general purpose computer and computer readable medium

providing the method in order to provide cost affective changes and upgrades to the system (Official Notice). It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the apparatus of Hasegawa and Hamadani with computer readable medium in order to provide a general purpose computer the method to perform the decoding process (Official Notice).

Claims 21, 23-26, 30-34 and 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa and Hamadani as applied to claim 20 above, and further in view of US Patent 5,363,097 to Jan.

[claims 21, 23-26 and 30-34]

Hasegawa and Hamadani teach the apparatus of claim 20 as shown above. Hasegawa and Hamadani do not teach the use of a two way buffering between each stage of the decoding process. Jan teaches the use of a controlled data buffer for reading and writing data between the different stages of the decoding process in order to satisfy a system data rate (Col 5 Lines 58-68, Col 6 Lines 1-10, Fig. 3-5). Though Jan does not specifically say that the buffer controller is DMA, DMA is well know in the art (Official Notice). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the decoder of Hasegawa and Hamadani with the buffer system of Jan in order to satisfy a system's data rate requirements.

[claims 36 and 37]

As shown above for claims 1 and 7, Hasegawa and Hamadani teach the use the Huffman code format and DV format.

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa, Hamadani and Jan as applied to claim 30 in view of US Patent 6,496,199 to Peng et al.

[claim 35]

Hasegawa, Hamadani and Jan teach the use of a digital video decoder containing a preparser, vld, and a de-shuffler as shown above for claims 30. They do not teach the use of a Very Long Instruction Word (VLIW) processor. Peng teaches the use of a VLIW CPU to control a system-on-a-chip video decoder in order to implement an advanced multimedia system at an affordable cost and with a smaller footprint (Col 1 Lines 50-55, Lines 59-63). The VLIW CPU contains an on-chip instruction cache that could obviously be used to store instructions on preparsing video data. The steps of the decoder are obviously controlled under time sharing criteria because a real-time digital video decoder is required to perform the decoding steps in a specific amount of time. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the decoding method of Hasegawa and Hamadani with the system of Peng in order to produce an affordable and small advanced multimedia system.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent 5,929,794 to Hayakawa et al.

'Video Coding Application Design for Next Generation System-on-Chip Architectures' by Priebe et al.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erick Rekstad whose telephone number is 703-305-5543. The examiner can normally be reached on 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Kelley can be reached on 703-305-4856. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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